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# QUARTERLY TECHNICAL REPORT
**1st January 1993 - 31st March 1993**

GRANT NUMBER AND TITLE:# N00014-91-J-1441, "DLTS and Dynamic Transconductance Analysis of Deep-Submicron Fully- Depleted SOI MOSFET's"

GRANTEE:George Mason University;Dr.Dimitris E.Ioannou

SCIENTIFIC OFFICER:Dr. Alvin M. Goodman

## 1.PROGRESS THIS PERIOD

Progress this period was accomplished in two sepparate areas, namely hot electron degradation studies of partially and fully depleted transistors, and DLTS analysis to support gettering studies of various SOI SIMOX substrates.

The most interesting results on hot carrier degradation are summarized in the attached manuscript "Mechanisms of Hot-Carrier Induced Degradation of SOI(SIMOX) MOSFET's", to be presented at the forthcoming INFOS'93. Interesting results were also obtained on "Successive Charging/Discharging of Gate Oxides in SOI MOSFET's by Sequential Hot Electron Stressing of Front/Back Channel"The ability to inject hot-holes into the opposite gate oxide may be exploited for designing SOI flash memory cells with novel,back channel-based erasing schemes. Some of the expected advantages are reduced cell area, improved cell indurance characteristics, and short erase times (see attached draft).

Regarding DLTS Analysis of gettering effects, following several trial and error experiments, we have now established the most usefull device structure,a schematic of which is attached on this report.

Some of our work on SOI MOSFET Physics,dealing with the value of the surface potential at threshold in fully depleted devices,will appear in the June 1993 issue ofIEEE Transactions on Electron Devices (copy attached), and a full length paper on the mechanisms of our hot carrier degradation studies is under preparation for IEEE Transactions on Electron Devices.

Two research students are working on the project,Mr Andre Zaleski and Mr. Sinha Shankar.

## 2.PLANS FOR NEXT PERIOD

(a) Continue the study of hot-carrier degradation mechanisms,and complete a manuscript for submission to IEEE Trans.on Electron Devices.

(b) Continue the work on accumulation mode, fully depleted devices supplied by IBM and compare depletion mode technologies.

(c) Conduct DLTS studies on gettered SOI wafers on devices supplied by NRL.

## 3.POTENTIAL PROBLEM AREAS

(a) Technical:None

(b) Funding:None

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# Mechanisms of Hot-Carrier Induced Degradation of SOI (SIMOX) MOSFET's

A. Zaleski[a], D.E. Ioannou[a], G.J. Campisi[b], and H.L. Hughes[b]

[a]Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030†

[b]Naval Research Laboratory, Washington, D.C. 20375

An experimental study of the degradation mechanisms of hot-carrier stressed SOI (SIMOX) MOSFET's is carried out. Depending on the applied stress conditions, it is found that device degradation is mainly caused by electron and hole trapping by intrinsic and generated oxide traps and/or by generation of interface states. Sequential hot-electron stressing of the front/back channels results in successive electron/hole injection in the gate oxides, leading to important insights on the nature of the degradation mechanisms.

## 1. EXPERIMENTAL

The sample selection and stress conditions were designed to investigate (a) the relative importance of interface state generation versus oxide charge trapping, (b) the back channel degradation induced during front channel stressing and vice versa, and (c) the effects of oxide traps introduced in the drain region by the LDD implants.

Four lots of partially-depleted (PD) and two lots of fully-depleted (FD) SIMOX transistors were studied. The SIMOX wafers were prepared by oxygen implantation and high-temperature annealing in an argon ambient. The buried oxide thickness was 400 nm and the front gate oxide 15-20 nm. The film thickness and doping were 300 nm and $2\times10^{17}$ cm$^{-3}$ for the PD and 140 nm and $4\times10^{16}$ cm$^{-3}$ for the FD transistors. The devices studied were n-channel MOSFET's which incorporated LDD's of varying design and body ties to the source to reduce the floating body effects. The channel lengths were 0.6, 0.8, 1.0, 1.2 and 1.4 $\mu$m.

Suitable bias levels were applied for electron injection (EI) and/or hole injection (HI) conditions in the front channel whereas only EI conditions could be achieved for the back channel. In all cases, the opposite channel was kept in accumulation. The degradation was monitored by measuring the static transistor characteristics, and more detailed analysis was made by dynamic transconductance measurements and PISCES simulations.

†The work at George Mason University is supported by DNA through ONR Grant # N00014-91-J-1441.

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## 2. RESULTS

Using dynamic transconductance [1], the entire forbidden gap (from accumulation through depletion to inversion) can be probed with high sensitivity and resolution by making the measurement first with the current flowing through the channel next to the interface under investigation and then through the opposite channel. The required surface potential value is obtained by suitable monitoring of the drain current changes with the applied biases. For unstressed devices U shaped $D_{it}(E)$ profiles were obtained with interface state densities ranging from mid $10^{11}$ $cm^{-2}$ $eV^{-1}$ near the middle of the band gap to upper $10^{12}$ $cm^{-2}$ $eV^{-1}$ near the band edges for both interfaces, for channel lengths down to 0.6 $\mu$m (Figure 1). Following stress, $D_{it}$ increased considerably in the case of the HI conditions (Figure 1), but remained almost unchanged in the case of EI conditions

Static characteristics of stressed transistors indicated significant charge trapping in the gate oxides for all cases studied [2][3][4]. It has not always being easy to distinguish between interface and oxide charges, and along with dynamic transconductance measurements, extensive PISCES simulations were also conducted. For instance, charges trapped in the oxide just above/below the drain and channel areas were found by simulations to affect the transistor characteristics in a fashion similar to the effects of the channel interface states (Figure 2). Such traps may well be introduced in the spacer layer above the drain and/or in the buried oxide below the drain during the LDD fabrication process, and could carelessly be misinterpreted as interface states in the channel.

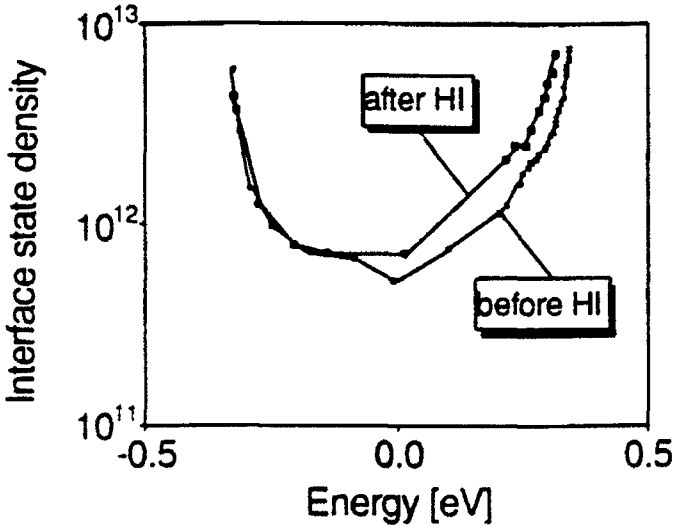


Figure 1.Typical $D_{it}$ vs. energy profile before and after hot-hole stress (HI).

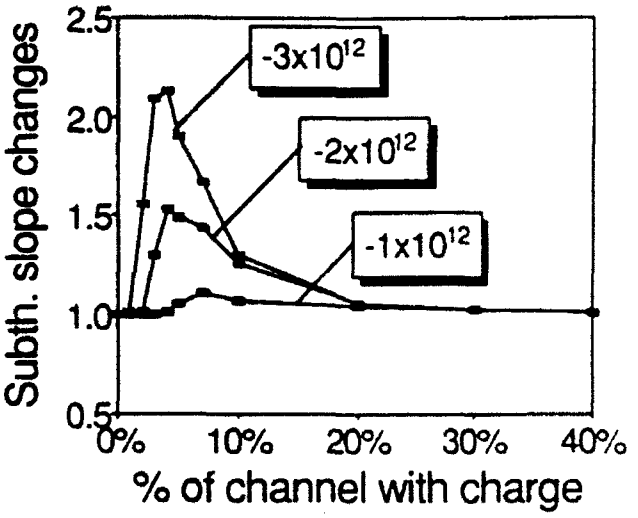


Figure 2. Simulated subthreshold slope vs. negative interface charge density and extent of localization above the channel near the drain.

Figures 3 and 4 show the results of sequential front EI/back EI and front HI/back EI stressing, respectively. In Figure 3 it is seen that front EI conditions (I, II, IV, VI) degrade

transistor parameters substantially, which then fully recover during the subsequent back EI (III, V). This would suggest that the electron trapping occurring in the front gate oxide during front EI is completely compensated by hole trapping during the following back EI. This is also a strong evidence of very efficient hot-hole injection into the interface opposite to that under stress, which could be used in novel erasing schemes for flash memories [5]. In Figure 4 it is seen that front HI conditions (I, III, V) cause damage that does not recover by the hole injection resulting from back EI (II, IV) stressing as far as the subthreshold

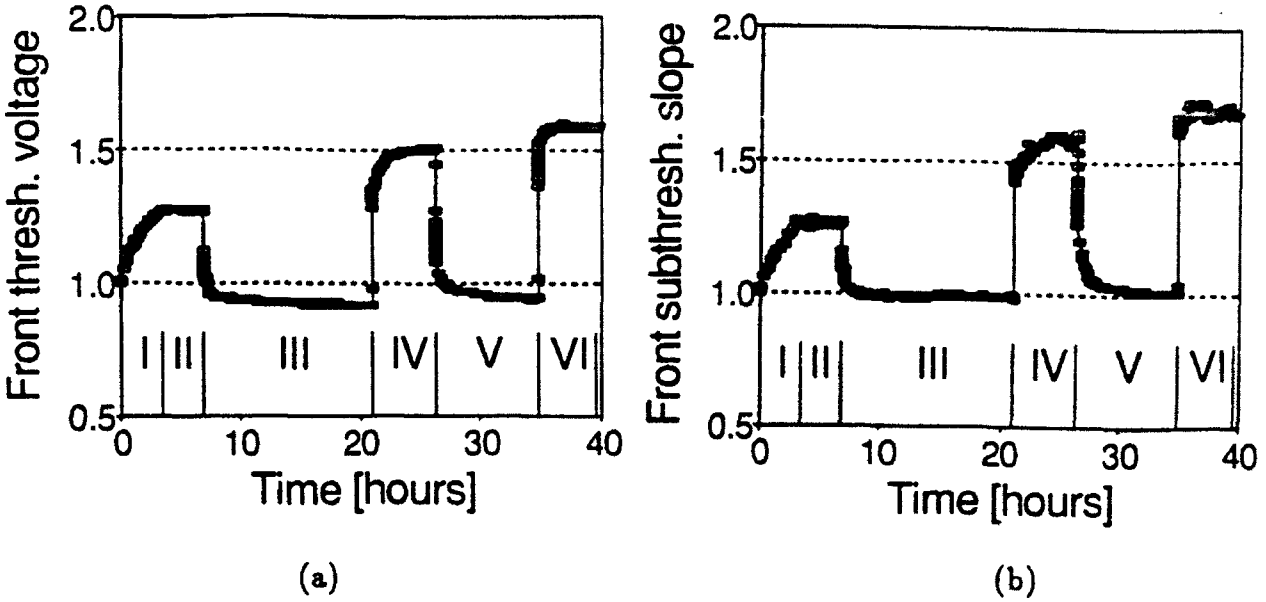


Figure 3. Front channel threshold voltage (a), and subthreshold slope (b) changes during sequential front/back channel hot-electron stress (EI).

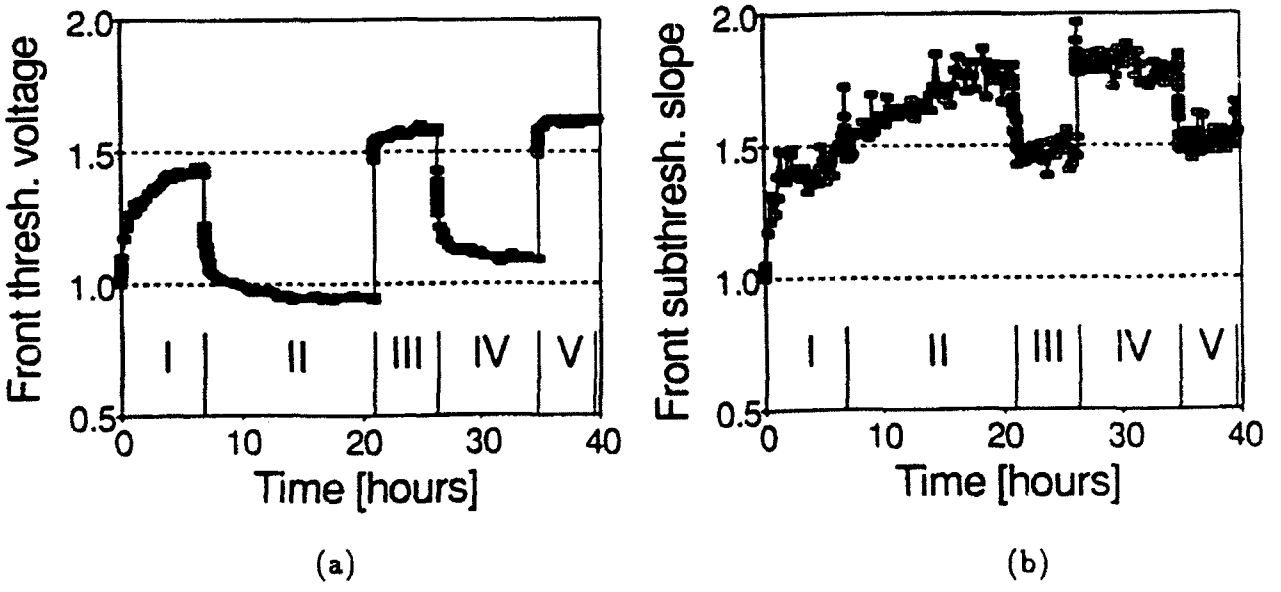


Figure 4. Front channel threshold voltage (a), and subthreshold slope (b) changes during sequential front HI/back EI stress.

slope is concerned. This hole injection, however, causes the front threshold voltage (Figure 4a) to decrease significantly. This indicates that during front HI stressing, along with holes, electrons are also injected into the front oxide, and a considerable amount of interface states are generated. More detailed analysis of the time rates of the degradation characteristics in Figure 3 provides evidence of a two-step degradation process, consisting of oxide trap creation followed by oxide trap filling.

## 3. CONCLUSIONS

The main conclusions can be summarized as follows: (i) the main cause of degradation is oxide charges trapped by intrinsic and/or induced oxide traps. However, dynamic transconductance measurements produced evidence of significant interface state generation in some cases, under HI conditions. Additional support for this conclusion was obtained by numerical simulations as well as from the nature of the degradation observed during sequential front/back gate stressing; (ii) charges trapped in the oxide just above/below the drain were found by PISCES simulations to affect the transistor characteristics in a fashion commonly attributed to the channel interface states; (iii) stressing one channel under EI/HI conditions results in hot-hole injection into the opposite channel and provides a good criterion to separate the processes of charge trapping and interface state generation; (iv) this possibility to inject hot-holes into the opposite channel may be utilized to design back-channel-based erasing schemes for flash memories.

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Draft

# Successive Charging/Discharging of Gate Oxides in SOI MOSFET's by Sequential Hot Electron Stressing of Front/Back Channel.

Andrzej Zaleski, *Student Member, IEEE*, Dimitris E. Ioannou, *Member, IEEE*,
George J. Campisi[1], *Member, IEEE*, and Harold L. Hughes[1], *Member, IEEE*,

Department of Electrical and Computer Engineering
George Mason University, Fairfax, VA 22030

[1] Naval Research Laboratory, Washington, D.C. 20375

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**Abstract**

Hot-hole injection into the opposite channel of SOI MOSFET's under hot-electron stress is reported. Sequential front/back channel hot-electron stressing results in successive hot-electron/hole injection, causing the threshold voltage to increase and decrease accordingly. The ability to inject hot-holes into the opposite gate oxide, may be exploited for designing SOI flash memory cells with novel, back-channel-based erasing schemes. Some of the expected advantages are reduced cell area, improved cell endurance characteristics, and short erase times.

## 1. Introduction

As progress is being continuously made on various SOI technologies there is much current interest on studies aimed at exploiting the unique properties exhibited by MOSFET devices made by these technologies for VLSI applications [1]. Especially important in this regard is the ability to bias the front and the back gate independently, and the interaction of these two gates. This interaction may, for example, take the form of electrostatic coupling in fully-depleted devices and affect the observed threshold voltage [2], subthreshold swing [3][4], and transconductance [4]. It may also result in degradation of a channel during hot carrier stressing of the opposite channel. However, opinion varies as to whether the opposite channel sustains actual damage, or it appears to be degraded through electrostatic coupling [5][6][7][8][9]. The purpose of this letter is to demonstrate that stressing one channel can in fact inject charges into the other channel,and to point out that this could have important device applications, such as write/erase schemes for flash memories, for instance [10].

## 2. Experimental

In this work, both partially depleted (PD) and fully depleted (FD) SOI MOSFET's, fabricated on high temperature annealed SIMOX wafers were investigated. The buried oxide thickness was 400 nm and the front gate oxide 15-20 nm. The film thickness and doping were 300 nm and $2\times10^{17}$ cm$^{-3}$ for the PD and 140 nm and $4\times10^{16}$ cm$^{-3}$ for the FD transistors. The devices studied were n-channel MOSFET's which incorporated LDD's of varying design and body ties to the source to reduce the floating body effects. The channel length varied from 0.6 to 1.4 $\mu$m.

The channels were sequentially stressed under hot-electron injection conditions, while the opposite channel was kept in accumulation. The transistor static characteristics were monitored with an HP4145B parameter analyzer throughout the stressing by briefly interrupting to take the measurement.

## 3. Results and Discussion

Figures 1 and 2 show results obtained for a 0.8 $\mu$m channel length PD device, which was sequentially stressed for two hours under front channel hot-electron injection conditions (FEI),

followed by two hours of back channel hot-electron injection conditions (BEI), and repeating the cycle for a total of twenty eight hours. During the front channel stress the source was grounded, the drain voltage was $V_D$=8 V, the front gate voltage was $V_{G1}$=8 V, and the back gate voltage was $V_{G2}$=-20 V, to keep the back interface accumulated. For the back channel the corresponding values were $V_D$=7.5 V, $V_{G1}$=-2 V, and $V_{G2}$=75 V.

Figure 1 shows the front channel static characteristics at the beginning of the third stress cycle (i.e. following BEI), in the middle of the cycle (i.e. following FEI), and at the end of the cycle (i.e. following BEI). It is seen that FEI degrade the characteristics substantially, which then recover fully during the subsequent BEI. This would suggest that the electron trapping occurring in the front gate oxide during FEI is completely compensated by hole trapping during the following BEI stress. This is seen more clearly in Fig.2(a) and (b), where the front and back threshold voltage $V_{T1}$ and $V_{T2}$ variations (normalized to the corresponding values for the unstressed transistor) are plotted with time throughout the entire stress duration. During the first FEI electron trapping in the front gate oxide causes $V_{T1}$ to quickly increase by more than 60% of its pre-stress value (Fig.2(a)). During the BEI stressing which immediately follows, $V_{T1}$ drops quickly back to its initial value. In the cycles that follow, $V_{T1}$ increases during FEI to a value slightly higher than the previous maximum, and decreases during BEI down to a value slightly higher than the previous minimum, such that the difference $V_{T1max}$ - $V_{T1min}$ remains constant. The situation is similar for the back channel, where $V_{T2}$ increases during BEI and decreases during FEI. The results shown above are typical of both PD as well as FD devices, in the sense that similar threshold voltage variations with time were observed.

The hot-holes injected into the opposite gate oxide are generated by impact ionization in the channel under stress, and in bulk devices they would normally contribute to the substrate current [11]. In the present structures however, due to the short distance, they can reach the opposite interface and move into the dioxide, aided by the favorably directed electric field. It should be noted at this point that the gate voltage used to keep the opposite channel accumulated was small enough not to cause electron detrapping, which was verified by additional experiments. Also, the full recovery of the transistor characteristics at the end of each stress cycle (Fig.1), suggests that

no interface state generation is involved.

This ability to inject hot holes into the opposite gate oxide has an important implication for a potential device application. More specifically, it could be utilized for designing a SOI based flash memory cell, with a back channel based erasing scheme. Erasing by hot-hole injection from the back interface does not involve large electric fields across the front gate oxide or along the front channel, and this should improve the cell endurance characteristics. If front channel electron injection (FEI) is used to program the cell, the holes during the (BEI based) erase cycle will be directed towards the region where the electrons were injected during programming. This should improve the erasing efficiency, shorten the erase time, reduce the possibility of over-erasure, and eliminate uncompensated front oxide electron trapping. Because of the "built-in" nature of the erase scheme, the cell area should be reduced. An apparent disadvantage of the cell would be the large back gate voltage values. This, however, is less significant if FD transistors and thinner back gate oxides are used. SIMOX buried oxides of thickness down to 100 nm, for example, are expected to become available in the near future [12].

## 4. Conclusions

Successive hot-electron/hole injection in the gate and buried oxides of SOI MOSFET's is achieved by sequential hot-electron stressing of front/back channel. Hot-electron injection increases the threshold voltage of the corresponding channel substantially, and the subsequent hot-hole injection brings the threshold voltage back to its original value. This possibility to inject hot-holes into the opposite channel can be utilized to design SOI-based flash memory cells with novel erasing schemes.

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## Figure captions

Fig 1: Static $I_D$ vs. $V_{G1}$ characteristics of a 0.8 $\mu$m channel length PD transistor, at the beginning, middle, and the end of the third stress cycle, following hot-electron stressing of the back, front and back channel, respectively. $V_D$=0.1 V, and $V_{G2}$=-20 V.

Fig 2: Front (a) and back (b) threshold voltages, normalized to their prestress values, throughout the duration of stress (seven stress cycles) for the same device as in Fig.1.

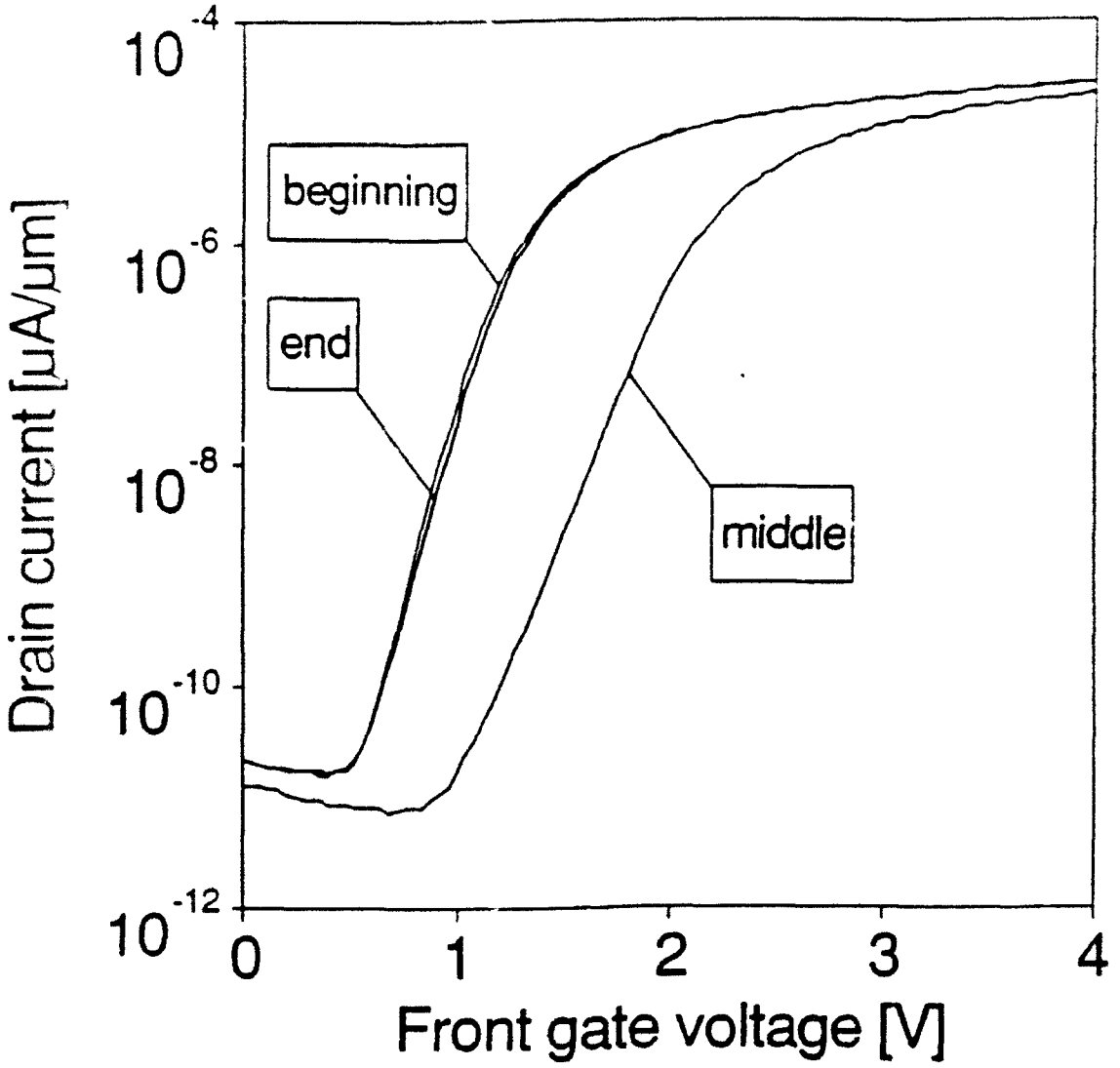
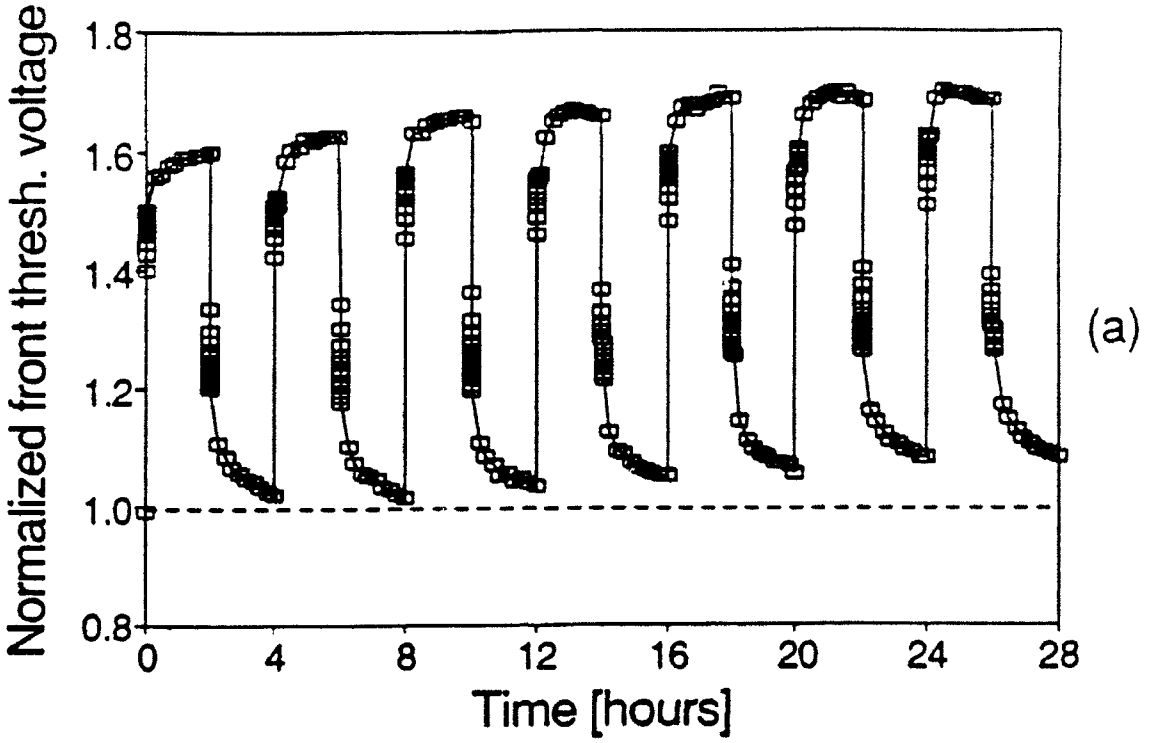

Drain current [μA/μm]
10^-4
10^-6
10^-8
10^-10
10^-12
beginning
end
middle
0
1
2
3
4
Front gate voltage [V]

Fig.1


Normalized front thresh. voltage
1.8
1.6
1.4
1.2
1.0
0.8
0
4
8
12
16
20
24
28
Time [hours]
(a)

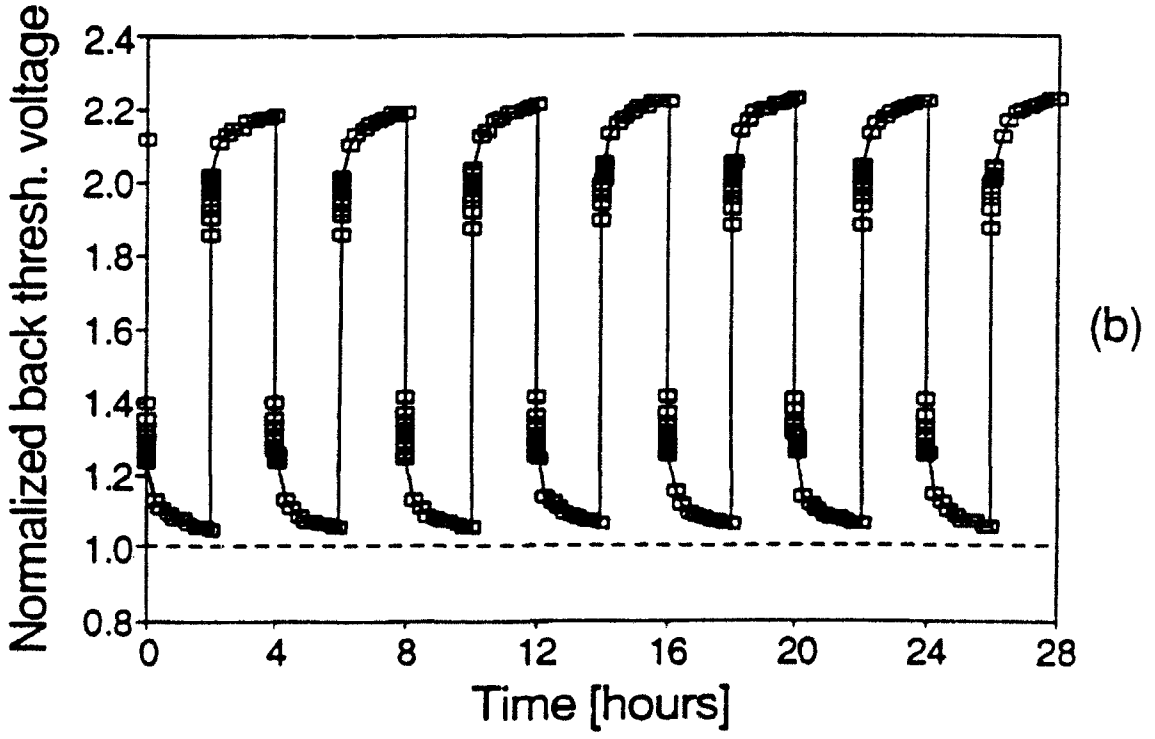

Normalized back thresh. voltage
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0
4
8
12
16
20
24
28
Time [hours]
(b)

Fig.2

# Surface Potential at Threshold in Thin-Film SOI MOSFET's

Baquer Mazhari and Dimitris E. Ioannou, *Member, IEEE*

*Abstract*—**The usual condition for threshold in bulk MOSFET's, of equal rates of change with gate voltage of the inversion and bulk charges, is suitably modified to describe threshold in fully depleted SOI MOSFET's. Using this modified condition the value of the surface potential at threshold in fully depleted transistors is obtained analytically in terms of device dimensions, film doping level, and applied voltages. The results are in excellent agreement with one-dimensional numerical simulations, and it is shown that the surface potential at threshold may differ significantly from $2\phi_F$, the value conventionally assumed.**

## I. Introduction

INTEREST in ultra-thin, fully depleted (FD) silicon-on-insulator (SOI) MOSFET's has been growing recently at a rapid rate, as their many unique properties are being increasingly recognized [1], [2]. The silicon film (typically less than 100 nm) is fully depleted of free carriers during the operation of these devices. This leads to a strong electrical coupling of the two interfaces and results in interesting behavior of the threshold voltage [3], the subthreshold current [4], [5], and the transconductance [5] characteristics. It also leads to challenging problems regarding electrical characterization of the bulk of the film [6], [7] and the interfaces [8].

In this paper we consider further the threshold voltage of these transistors and in particular the value of the surface potential at threshold. Following the early work of Brown [9], Linder [10], and others [11], [12] it has been widely accepted to define the threshold voltage of relaxed geometry bulk MOSFET's as the gate voltage at which the surface potential is $2\phi_F$, where $\phi_F$ is the bulk Fermi potential. Subsequent work [13], [14] re-enforced this definition, and although departures (sometimes serious) from $2\phi_F$ are observed [15], this value continues to serve analytical studies of bulk MOSFET's quite well [16], [17]. Following bulk silicon practice, the same $2\phi_F$ value of the surface potential at threshold has been assumed to be true for SOI MOSFET's as well [3] and is used widely in the literature [2]. However, serious problems with this assumption have been identified [18], [19] in thin-film SOI MOSFET's. As the trend in SOI technology continues to be towards such thin-film devices [1], [2], it is important to take a closer look at the value of surface potential at threshold and re-examine the above assumption.

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B. Mazhari is with the Department of Electrical Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801.

D. E. Ioannou is with the Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030.

IEEE Log Number 9208282.

## II. Basic Model

For bulk MOSFET's, the use of $2\phi_F$ as surface potential implies that the threshold voltage corresponds to a condition where the gate voltage modulates the inversion ($Q_i$) and depletion ($Q_D$) charges equally, i.e., the inversion ($C_i = dQ_i/d\phi_s$) and depletion ($C_D = dQ_D/d\phi_s$) capacitances are equal [11], [12]

$$\frac{dQ_i}{d\phi_s} = \frac{dQ_D}{d\phi_s} \tag{1}$$

Noting [11] that near threshold the depletion charge $Q_D = \epsilon_s E_s$, where $E_s$ is the electric field at the Si–$SiO_2$ interface, the threshold condition can be written in a more general form as

$$C_i = \epsilon_s \frac{dE_s}{d\phi_s}. \tag{2}$$

This expression is more appropriate for thin-film SOI MOSFET's where the silicon film gets fully depleted at gate voltages lower than the corresponding bulk threshold voltage, and the depletion charge remains constant at a value determined by the film thickness and doping. The electric field $E_{s1}$ at the front Si–$SiO_2$ interface, however, changes with the gate voltage and it can be easily shown that for a fully depleted silicon film

$$\Delta E_{s1} = \frac{\Delta\phi_{s1} - \Delta\phi_{s2}}{t_{Si}} = \frac{C_{ox2}}{C_d + C_{ox2}} \frac{\Delta\phi_{s1}}{t_{Si}} \tag{3}$$

where $\phi_{s1}$ and $\phi_{s2}$ are the potentials at the front and buried Si–$SiO_2$ interfaces, respectively, $t_{Si}$ the film thickness, $C_d = \epsilon_s/t_{Si}$ the film capacitance, and $C_{ox2}$ the capacitance of the buried oxide. Using (2) and (3), the threshold condition can thus be written as

$$C_i = \frac{C_d C_{ox2}}{C_d + C_{ox2}}. \tag{4}$$

The inversion charge density can be expressed in terms

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of usual parameters as

$$Q_i = q\frac{n_i^2}{N_A}\int_{\phi_{s1}}^{\phi_{s2}} \exp(\beta\phi)\frac{dx}{d\phi}\,d\phi. \tag{5}$$

Differentiating this equation with respect to $\phi_{s1}$, the inversion capacitance can be expressed as

$$C_i = q\frac{n_i^2}{N_A}\left\{\frac{\exp(\beta\phi_{s1})}{E_{s1}} - \frac{C_d}{C_d + C_{ox2}}\frac{\exp(\beta\phi_{s2})}{E_{s2}}\right\} \tag{6}$$

where $E_{s2}$ is the electric field at the back interface. The surface potential and electric field at the buried interface can be expressed as

$$E_{s2} = E_{s1} - \frac{q}{\epsilon_s}N_A t_{Si} \tag{7}$$

$$\phi_{s2} = \phi_{s1} - E_{s1}t_{Si} + \frac{q}{2\epsilon_s}N_A t_{Si}^2. \tag{8}$$

Substituting (6)–(8) in (4), the surface potential at threshold can now be expressed as

$$\phi_{s1}' = \phi_F + \frac{kT}{q}\ln\left\{\frac{\frac{C_dC_{ox2}}{C_d + C_{ox2}}E_{s1}}{qn_i f}\right\} \tag{9}$$

where

$$f = 1 - \left(\frac{C_d}{C_d + C_{ox2}}\right)\left(\frac{E_{s1}}{E_{s1} - \frac{q}{\epsilon_s}N_A t_{Si}}\right) \cdot \exp\left\{-\beta\left(E_{s1}t_{Si} - \frac{q}{2\epsilon_s}N_A t_{Si}^2\right)\right\} \tag{10}$$

and (by using the Gauss's law at the front and the back interface and letting $V_{G2}$ be the backgate voltage)

$$E_{s1} = \frac{C_dC_{ox2}}{C_d + C_{ox2}}\frac{\phi_{s1} - V_{G2}}{\epsilon_s} + \frac{qN_A t_{Si}}{2\epsilon_s}\left(1 + \frac{C_d}{C_d + C_{ox2}}\right). \tag{11}$$

Fig. 1 compares the surface potential determined from the analytical model (i.e., (9)) with $2\phi_F$ and the results obtained from a one-dimensional (1D) numerical solution of the Poisson equation [20] for different doping levels and $V_{G2} = -1$ V. Typical values of $t_{ox1} = 250$ Å, $t_{ox2} = 5000$ Å, and $t_{Si} = 500$ Å were assumed. Numerically, the threshold voltage and the corresponding surface potential were obtained as in [19] by applying the linear extrapolation method to $Q_i$ versus $V_{G1}$ characteristics in strong inversion. It is seen from this figure that the surface potential obtained from the analytical model tracks the numerically determined values very well but with an almost constant negative offset of 0.11 V.

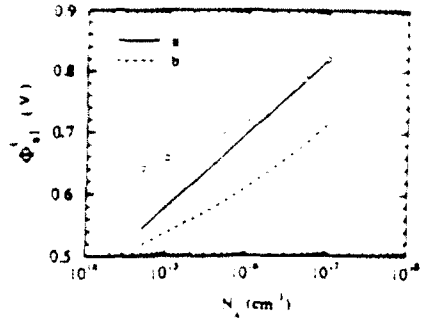


Fig. 1. Variation of surface potential at threshold ($\phi_{s1}'$) with the film doping ($N_A$). Curve *a* was obtained for surface potential of $2\phi_F$, curve *b* was obtained from the analytical model (9), and the circles denote the numerically determined values. Back-gate voltage was $V_{G2} = -1$ V. The front-gate oxide, silicon film, and buried oxide thicknesses were 250, 500, and 5000 Å, respectively.

## III. Model Refinement and Discussion

The discrepancy of 0.11 V in surface potential obtained from the analytical and numerical model implies that the threshold condition described by (4) is closer to subthreshold regime than inversion. It will now be argued that an estimate of proximity of the device to strong inversion can be obtained by computing the parameter

$$\alpha = \frac{1}{C_{ox1}}\frac{dQ_i}{dV_{G1}}.$$

This parameter has a value of zero deep in the subthreshold region and unity in strong inversion. For the threshold condition described by (4), $\alpha$ can be determined as follows: application of Gauss's law at the front Si–$SiO_2$ interface gives

$$\epsilon_{ox}\frac{\Delta V_{G1} - \Delta\phi_{s1}}{t_{ox1}} - \epsilon_s\Delta E_{s1} = \Delta Q_i \tag{12}$$

or

$$\Delta V_{G1} = \frac{\Delta Q_i}{C_{ox1}} + \epsilon_s\frac{\Delta E_{s1}}{C_{ox1}} + \Delta\phi_{s1} \tag{13}$$

and substituting $E_{s1}$ from (3)

$$\Delta V_{G1} = \frac{\Delta Q_i}{C_{ox1}} + \Delta\phi_{s1}\left\{1 + \frac{C_dC_{ox2}}{C_{ox1}(C_d + C_{ox2})}\right\}. \tag{14}$$

Noting that $\Delta\phi_{s1} = \Delta Q_i/C_i$ and substituting (4) in the above expression, $\alpha$ can be expressed as

$$\alpha = \frac{1}{C_{ox1}}\frac{dQ_i}{dV_{G1}} = \frac{C_dC_{ox2}}{2C_dC_{ox2} + C_{ox1}C_d + C_{ox1}C_{ox2}}. \tag{15}$$

For $t_{ox1} = 250$ Å, $t_{ox2} = 5000$ Å and $t_{Si} = 500$ Å, $\alpha = 0.0238$ is obtained, suggesting that the threshold condition described by (4) occurs well into the subthreshold region. Since $\alpha$ varies from 0 to 1 as the transistor moves from the deep subthreshold regime to strong inversion, one might seek to define threshold to be the gate voltage at which $\alpha = 0.5$. Physically, this represents the onset of linearity in the charge control relationship. This can be understood from the fact that in the subthreshold region,

the charge control relationship is exponential and

$$\Delta V_{G1} \simeq \frac{\epsilon_s \Delta E_{s1}}{C_{ox1}} + \Delta\phi_{s1}$$

while, in strong inversion, the charge control is linear and

$$\Delta V_{G1} = \frac{\Delta Q_i}{C_{ox1}}.$$

When both the linear and nonlinear contributions in the charge control law are equal

$$\frac{\Delta Q_i}{C_{ox1}} = \frac{\epsilon_s \Delta E_{s1}}{C_{ox1}} + \Delta\phi_{s1}. \tag{16}$$

From (13) and (16), it is easily seen that this condition corresponds to $\alpha = 0.5$. On substituting (3) in (16), the new threshold condition and the corresponding surface potential can be written as

$$C_i = \frac{C_d C_{ox2}}{C_d + C_{ox2}} + C_{ox1} \tag{17}$$

$$\phi'_{s1} = \phi_F + \frac{kT}{q} \ln\left\{\frac{\dfrac{C_d C_{ox2}}{C_d + C_{ox2}} E_{s1}}{qn_i f}\right\} + \frac{kT}{q} \ln\left\{1 + \frac{C_{ox1}(C_d + C_{ox2})}{C_d C_{ox2}}\right\}. \tag{18}$$

Equation (18) adds only a fixed offset to the expression for surface potential derived earlier (see (9)). It is interesting to note at this point that the condition $\alpha = 0.5$ can be shown to lead to the definition of threshold introduced by McKitterick and Caviglia [19]: with the symbols having their usual meanings, constant mobility and $\alpha = 0.5$, one can write

$$\frac{dQ_i}{dV_{G1}}\,(\text{threshold}) = \frac{1}{2} C_{ox1} \tag{19}$$

$$\mu \frac{W}{L} V_D \frac{dQ_i}{dV_{G1}}\,(\text{threshold}) = \frac{1}{2} \mu \frac{W}{L} V_D C_{ox1} \tag{20}$$

$$\frac{d\left(\mu \dfrac{W}{L} V_D\right)}{dV_{G1}}\,(\text{threshold}) = \frac{1}{2} \frac{d}{dV_{G1}} \left(\mu \frac{W}{L} V_D C_{ox1}\right) \tag{21}$$

$$\frac{dI_D}{dV_{G1}}\,(\text{threshold}) = \frac{1}{2} \frac{dI_D}{dV_{G1}}\,(\text{large } V_{G1}). \tag{22}$$

The last equation is identical to [19, eq. (14)] which McKitterick and Caviglia used to define threshold, and it is thus seen that the physical basis of that rather arbitrarily introduced definition [19] is the same as the one used here, i.e., equal linear and nonlinear contributions in the charge control law. Fig. 2 shows a comparison of surface potential obtained from the new definition of threshold and numerically calculated values. The agreement is very good but there still remains an offset of about 14 mV.

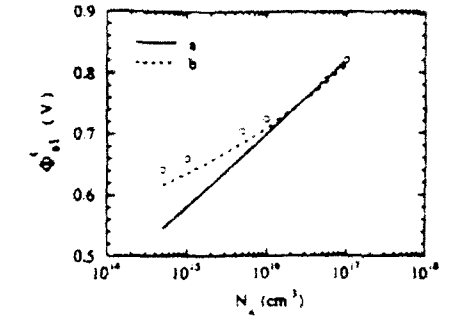


Fig. 2. Variation of surface potential at threshold ($\phi'_{s1}$) with the film doping ($N_A$). Curve *a* corresponds to surface potential of $2\phi_F$, curve *b* was obtained from the improved analytical model (18), and the circles denote the numerically determined values. $V_{G2}$ and device dimensions same as in Fig. 1.

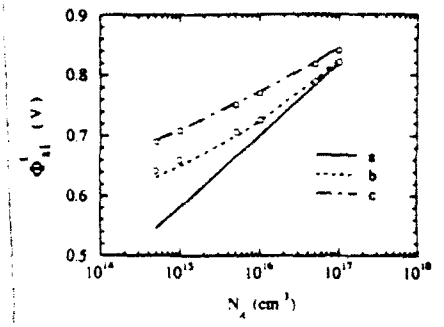


Fig. 3. Variation of surface potential at threshold ($\phi'_{s1}$) with the film doping ($N_A$). Curves *b* and *c*, corresponding to back-gate voltages of $-1$ and $-15$ V, respectively, were obtained using the analytical model (24) with $\alpha = 0.63$. Curve *a* corresponds to surface potential of $2\phi_F$ while the circles and squares denote the numerically determined values. Device dimensions same as in Fig. 1.

To examine this remaining offset further, the numerically obtained $Q_i(V_{G1})$ plots were used to evaluate $\alpha$ at the corresponding threshold voltage (obtained by linear extrapolation). It was found that $\alpha$ remained constant at $\alpha \approx 0.63$ to within 2% for front gate oxide thicknesses, silicon film thicknesses, and doping levels in the range 100–250 Å, 500–1500 Å, and $10^{15}$–$10^{17}$ cm$^{-3}$, respectively. For an arbitrary $\alpha$, (17) can be generalized to

$$C_i = \frac{\alpha}{1 - \alpha}\left(C_{ox1} + \frac{C_d C_{ox2}}{C_d + C_{ox2}}\right) \tag{23}$$

and the corresponding surface potential can be expressed as

$$\phi'_{s1}(\alpha) = \phi'_{s1}(\alpha = 0.5) + \frac{kT}{q} \ln \frac{\alpha}{1 - \alpha}. \tag{24}$$

Letting now $\alpha = 0.63$, Fig. 3 shows the comparison of the analytical model described by (24) with the numerically calculated values for $V_{G2} = -1$ and $-15$ V. An excellent fit is obtained at both the back-gate voltages and for all doping levels, demonstrating the validity of the model.

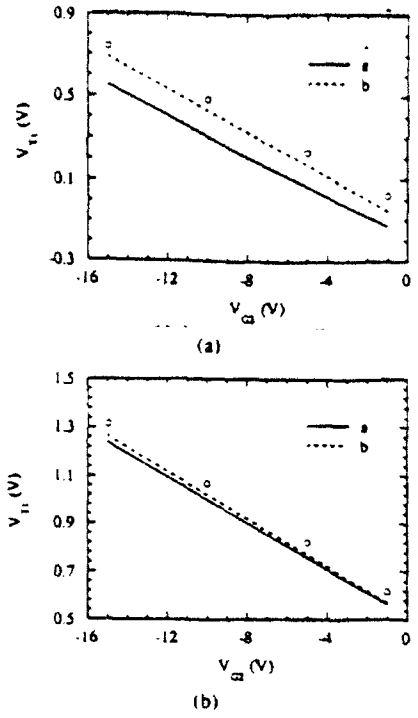


Fig. 4. Variation of threshold voltage with the backgate voltage for a film doping of $10^{15}$ cm$^{-3}$ (a) and $10^{17}$ cm$^{-3}$ (b). Curve *a* was obtained for surface potential of $2\phi_F$, curve *b* was obtained by using a value of surface potential obtained from our analytical model (24), and the circles represent the numerically determined values. Device dimensions same as in Fig. 1.

## IV. Threshold Voltage

The expression for threshold voltage can be written as

$$V_{Th} = V_{FB} + \phi'_{s1}(\alpha) + \frac{\epsilon_s E_{s1}}{C_{ox1}} \qquad (25)$$

where $V_{FB}$ is the flatband voltage, here taken to be equal to the work-function difference between the n$^+$ polysilicon gate and the silicon film. Fig. 4 shows a comparison of the threshold voltage obtained from our model using $\alpha = 0.63$, numerically calculated values, and threshold voltage determined for surface potential of $2\phi_F$. Our model tracks the threshold voltage very well. There is a small offset due to neglect of inversion charge at threshold in the expression for the electric field $E_{s1}$ at the front interface.

## V. Conclusions

Analytical expressions for the surface potential at threshold in fully depleted MOSFET's have been obtained, which are in excellent agreement with one-dimensional numerical simulations. The value of this potential depends on device geometry, film doping, and applied voltages, and may be significantly different than $2\phi_F$, especially for lowly doped and thin films. By considering the interrelationships of various physical quantities of significance in the operation of the fully depleted SOI MOSFET near threshold, we believe that a better conceptual understanding of the relevant surface condition of this device has been achieved. If the mobility changes due to electric field can be neglected, the above expressions should lead to more accurate threshold voltage values and interface state density versus energy profiles in current SOI technology development studies. This might be further explored by incorporating in the analysis various field-dependent mobility models.


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[20] The numerical calculations were performed with the software provided by J. B. McKitterick and A. L. Caviglia [19].

① Au. This is footnote material. Pls indicate where it belongs in text.

**Baquer Mazhari** was born in India on February 7, 1966. He received the B. Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, in 1987 and the M.S. degree in electrical engineering from the University of Maryland, College Park, in 1989.

He is at present studying towards the Ph.D. degree at the University of Illinois at Urbana-Champaign. His research interests include characterization and modeling of HBT's, III–V FET's, and thin-film SOI MOSFET's.

**Dimitris E. Ioannou** (M'82) was born in Limnohori, Serron, Greece, on May 27, 1951. He received the honors degree in physics from the University of Thessaloniki, Greece, in 1974 and the M.Sc. and Ph.D. degrees in solid-state electronics from the University of Manchester Institute of Science and Technology (UMIST), Manchester, England, in 1975 and 1978, respectively. His research there was mainly concerned with SEM-EBIC studies of boron-implanted silicon.

After graduating, he stayed on at UMIST and worked on DLTS of silicon crystals until 1979. From the Autumn of 1979 to December 1981, he was enlisted for National Service in the Greek Army, during which time he was also a Special Research Fellow at the Democritus University of Thrace, Greece, working on amorphous silicon solar cells. From January 1982 to August 1983, he was a Research Fellow in microelectronics at Middlesex Polytechnic, London, England. From August 1983 to December 1989, he was a faculty member of the Electrical Engineering Department, University of Maryland, College Park. In January 1990 he joined the faculty of George Mason University, Fairfax, VA, as an Associate Professor of Electrical and Computer Engineering, where he is teaching and conducting research in the areas of devices and materials for integrated circuits and optoelectronics.